

11. A circuit arrangement as claimed in claim 1, characterized in that the capacitive element (24) is constituted at least as a capacitor.

12. A circuit arrangement as claimed in claim 1, characterized in that an additional, fixed reference value is adjustable at the second input (34) of the threshold value circuit (30), particularly by means of an additional resistor.

13. A receiver, particularly a UHF or VHF receiver, comprising at least a subsequent circuit arrangement (100) as claimed in claim 1.

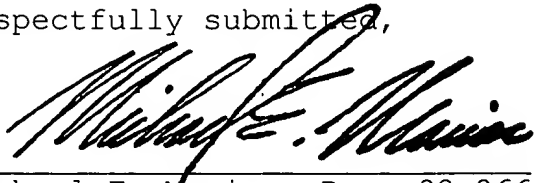
REMARKS

The foregoing Preliminary Amendment to claims 3-6, 8, and 10-13 were made solely to avoid filing the claim in the multiple dependant form so as to avoid the additional filing fee.

The claims were not amended in order to address issues of patentability and Applicant respectfully reserves all rights she may have under the Doctrine of Equivalents. Applicant furthermore reserves her right to reintroduce subject matter deleted herein at a later time during the

prosecution of this application or continuing applications.

Respectfully submitted,



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APPENDIX

3. A circuit arrangement as claimed in claim 1 [or 2], characterized in that the first input (32) of the threshold value circuit (30) is preceded by at least a filter stage (10).

4. A circuit arrangement as claimed in [any one of claims 1 to 3] claim 1, characterized in that the threshold level of the reference threshold signal adapts to the level of the input signal in the low-ohmic state of the resistor (22).

5. A circuit arrangement as claimed in [any one of claims 1 to 4] claim 1, characterized in that the threshold value circuit (30) is constituted by a comparator whose first input (32) is positive and whose second input (34) is negative.

6. A circuit arrangement as claimed in [any one of claims 1 to 5] claim 1, characterized in that the detector circuit (40) comprises at least a slope detector unit (42) and at least a clock regaining unit (44) connected to the slope detector unit (42), and in that the detector circuit (40) regenerates the data clock (f_{data}) from the digital output signal.

8. A circuit arrangement as claimed in [any one of claims 1 to 7] claim 1, characterized in that the control circuit (50) has an externally and/or internally triggerable reset function.

10. A circuit arrangement as claimed in claim 8 [or 9], characterized in that, after triggering the reset function of the control circuit (50), the capacitive element (24) is chargeable to a given capacitance (C_t).

11. A circuit arrangement as claimed in [any one of claims 1 to 10] claim 1, characterized in that the capacitive element (24) is constituted at least as a capacitor.

12. A circuit arrangement as claimed in [any one of claims 1 to 11] claim 1, characterized in that an additional, fixed reference value is adjustable at the second input (34) of the threshold value circuit (30), particularly by means of an additional resistor.

13) receiver, particularly a UHF or VHF receiver, comprising at least a subsequent circuit arrangement (100) as claimed in [any one of claims 1 to 12] claim 1.